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13. ABSTRACT (Maximum 200 words)

The objective of this Program is to develop long wavelength, lattice mismatched InGaAs PIN diode structures grown using Molecular Beam Epitaxy (MBE). The overall goal is to generate structures sensitive to the entire near infrared (1.0 - 2.5 μm) which take advantage of the uniformity inherent to MBE but with a buffer structure practical for commercialization. During Phase I we focused on an intermediate alloy, $In_{.74}Ga_{.26}As$, with response out to 2.2 μm. By the end of Phase I, PIN diodes were fabricated using thin (less than 3 μm), low-temperature linearly graded buffers (LTLGB) of $In_xGa_{1-x}As$. Shunt resistivities (RoA) > 75 Ω-cm^2, and peak quantum efficiencies > 70% were observed at room temperature. RoA had a temperature dependence with a diode quality factor of n=1.2. These results were near-commercial in level and represent the first practical alternative to non-uniform vapor phase epitaxy (VPE) material. During Phase II, the conventional planar process (zinc-diffused junctions through an InAsP cap) will be adapted to accommodate the MBE InAlAs cap, the opaque InGaAs LTLGB will be replaced by a transparent InAlAs buffer to enable backside-illuminated devices, and the indium content of the active layer will be increased to 82% for a cutoff wavelength of 2.5 μm.

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1. Project Summary (Phase I)

The objective of this Program is to develop long wavelength, lattice mismatched InGaAs PIN diode structures grown using Molecular Beam Epitaxy (MBE). The overall goal is to generate structures sensitive to the entire near infrared (1.0 - 2.5 μm) which take advantage of the uniformity inherent to MBE but with a buffer structure practical for commercialization. The activity during Phase I was centered on an intermediate alloy, $In_{.74}Ga_{.26}As$, with optical response out to 2.2 μm. By the end of Phase I, PIN diodes were fabricated using thin (less than 3 μm), low-temperature linearly graded buffers (LTLGB) of $In_xGa_{1-x}As$. The diodes had grown-in p-n junctions and InAlAs passivation caps. Shunt resistivities (RoA) > 75 Ω-cm^2, and peak quantum efficiencies > 70% were observed at room temperature. RoA had a temperature dependence with a diode quality factor of n=1.2. These results were near-commercial in level and represent the first practical alternative to non-uniform vapor phase epitaxy (VPE) material. During Phase II, (i) the conventional planar process (zinc-diffused junctions through an InAsP cap) will be adapted to accommodate the MBE InAlAs cap, (ii) the opaque InGaAs LTLGB will be replaced by a transparent InAlAs buffer to enable backside-illuminated devices, and (iii) the indium content of the active layer will be increased to 82% for a cutoff wavelength of 2.5 μm.

2. Program Objectives

2.1 Summary

The primary objective of this Program is to develop high quality, cost effective, large area optical sensors that cover the 1 - 2.5 μm near infrared. Commercial prototypes of these sensors are now made from InGaAs/InP material grown by vapor phase epitaxy (VPE). The spatial non-uniformity and expense of this material are significant drawbacks to large-scale commercialization. The relatively large size of one- and two-dimensional focal plane arrays, for example, demands very good uniformity. The very low yields achieved with VPE lead to reduced performance and high cost.

Our approach to growing the material for these detectors is to use molecular beam epitaxy (MBE) at Penn State. The primary benefit gained by using MBE as compared to VPE is the ability to grow epitaxial layers with excellent uniformity. Penn State reproducibly achieves compositional and electrical uniformity of about ±2% across a 3" wafer, comparable to commercial vendors of MBE material. In order to obtain the high quality epitaxial material required for state-of-the-art optical sensor arrays at wavelengths as long as 2.5 μm, we propose to use an unusually low substrate temperature to grow thin (< 2 μm) compositionally graded buffers which separate the active device layers from the substrate. This technique has been used successfully to produce high quality material on substrates which do not match the lattice constant of the epitaxial layer. Moreover, the low temperature graded buffer layers grown using this technique are thin (< 2 μm) in comparison to the graded buffer layers used by VPE (> 8 μm). Consequently, the relatively slower growth rate of MBE does not pose a fundamental obstacle to its commercial use.

To achieve optical sensitivity out to 2.5 μm requires an active layer of $In_{.82}Ga_{.18}As$. This material has a lattice constant 2% larger than the InP substrate. Thus the main technical task of this Program is to develop epitaxial techniques to grow high indium content lattice mismatched InGaAs on InP substrates with a material quality sufficient for good detectors. Reasonable-quality lattice-mismatched InGaAs grown by MBE for majority carrier devices with current flow parallel to the channel-active layer interface has been achieved; it has yet to be demonstrated for minority carrier devices with current flow through the interface. A corollary task is to adapt commercial planar processing technology designed for VPE wafers (junction diffusion through an InAsP cap) to the corresponding MBE wafer (InAlAs cap).

2.2 Phase I Technical Objectives (from Phase I Proposal)

Our objectives for Phase I of this program are to determine whether the use of low temperature graded buffer layers in a molecular beam epitaxy process can provide material suitable for improved commercially viable detectors and detector arrays in the 1.5 - 2.5 μm wavelength range. Equally important procedures to be compatible with the MBE material, and to identify what is needed to transfer the material growth technology to commercial suppliers. Specifically, we will:

1) Determine how epitaxial growth parameters such as substrate temperature, compositional grading rate, growth rate, and arsenic flux influence low temperature graded effectiveness, determined by p-n junction electrical properties.

2) Design an improved substrate measurement and control capability for MBE using optical transmission and reflectance, and perform key experiments to demonstrate its feasibility.

3) Determine how MBE material grown using low temperature linearly graded buffers compares with commercial VPE material and with MBE material grown using other buffer types.

4) Design epitaxial structures optimized for array detectors grown by MBE.

5) Determine what the key device processing issues are in fabrication of 1.5 - 2.5 μm diodes and detectors in material grown by MBE, using a mesa isolation process at Penn State, and a planar Zn-diffusion process at Sensors Unlimited.

6) Determine whether the low temperature linearly graded buffer approach or another related MBE epitaxial structure can deliver detectors which are commercially viable. Identify remaining problems of material growth and processing.

7) Determine whether commercial wafer vendors, using MBE growth, would be able to implement the growth at sufficiently low cost to be competitive.

Questions to be answered to determine feasibility of approach

The questions to be answered to determine the feasibility of our approach are:

1) Can the low temperature graded buffer approach using MBE be developed to grow material for 1.5 - 2.5 μm diodes with sufficiently low resistance-area products, low reverse bias leakage currents, and high current collection to be competitive with existing VPE material in terms of sensor performance?

2) Can the MBE growth process be controlled sufficiently well, especially regarding substrate temperature, to reproducibly obtain high quality material for sensors?

3) Can a device processing scheme be identified which has the potential for use with MBE material to give viable sensors at a reasonable cost?

4) Does the combination of the MBE material and device processing have the potential to compete favorably with existing material and processes in some segment of sensor production?

2.3 Phase I Work Statement (from Phase I Proposal)

Months	Task
0-2	Grow diode structures on linearly graded low temperature buffers by MBE, varying substrate temperature, grading rate, growth rate and arsenic flux.
1-4	Fabricate diode structures and optical sensors (in linearly graded low temperature buffered material grown by MBE) using mesa isolation.
2-5	Fabricate diode structures and optical sensors (in linearly graded low temperature buffered material grown by MBE) using Zn diffusion.
1-4	Perform electrical tests of diodes and electrical and optical tests of sensors fabricated by both the mesa isolation, concentrating on zero bias resistance-area product and reverse leakage current.
2-5	Perform electrical tests of diodes and electrical and optical tests of sensors fabricated by both the mesa isolation process at Penn State and the Zn diffusion process at Sensors Unlimited.
3-4	Identify a promising technique for improved substrate temperature control the MBE process at low substrate temperatures and perform feasibility experiments.
4-6	Design improved epitaxial structures for sensors fabricated from MBE material.
4-6	Compare the performance of diodes and sensors fabricated from MBE material to those fabricated from material commercially available, and asses the suitability of the MBE process for sensor material growth. Determine what work remains to be done for successful implementation of the process.

3. Work Carried Out/Results Obtained

3.1 Growth and Characterization of Diode Structures

3.1.1 Growth

For this study, all samples were grown in a Varian GEN-II MBE machine. A PIN diode with the epitaxial structure shown in Table 1 was chosen as a base line device. In particular, the structure consisted of a p^+ $In_{0.74}Ga_{0.26}As$ cap layer, a p^+ $In_{0.74}Al_{0.26}As$ window layer, and a one μm thick undoped active layer all grown on top of a compositionally graded $In_xGa_{1-x}As$ (x=0.53 to 0.74) n^+ buffer layer. Most of our effort focused on optimizing the buffer layer which will be described in this report. A 3000Å lattice matched n+ InGaAs buffer was inserted between the n+ InP substrate and the graded buffer to maximize the quality of the initiation of growth and allow the In furnace to come up to growth temperature. Because of the unusually low growth temperatures and improved surface morphologies demonstrated with As_2 versus As_4, As_2 was used for all growths. Moreover, the V/III flux ratio was maintained at 15 based on prior results obtained with lattice matched InGaAs.

To obtain device quality material in a relatively short period of time, the variation in growth parameters was limited to those shown in Table 2. Based on interim results, not all of the possible combinations in this matrix were investigated. Specific combinations will be discussed in the following sections.

In each case the graded buffer was divided into 50 equal segments and the concentration of indium was increased an equal amount at each step. Reducing the grade to a series of small steps approximates a linear increase in the indium composition with position. Because the indium composition must increase from 53% to 74%, a variation in buffer thickness from 0.5 μm to 2.0 μm corresponds to a grading rate of 40% In/μm to 10% In/μm.

The range of substrate temperatures, from 300°C to 400°C, was chosen based on an understanding that an increase in the indium composition should be matched with a decrease in the growth temperature to obtain high quality material. Lattice matched $In_{0.53}Ga_{0.74}As$ is typically grown near 500°C, therefore, our growth temperatures are considered relatively low which should allow for the high quality growth of $In_{0.74}Ga_{0.26}As$ active layers.

Table 1. Structure for baseline samples grown by MBE in Phase I.

Layer	Material	Thickness	Doping (cm^{-3})
Contact	$In_{0.74}Ga_{0.26}As$:Be	50 nm	5×10^{18}
Cap	$In_{0.74}Ga_{0.26}As$:Be	50 nm	5×10^{18}
Cap	$In_{0.74}Ga_{0.26}As$:Be	100 nm	6×10^{17}
Active	$In_{0.74}Ga_{0.26}As$	1.0 μm	undoped
n+ Buffer	$In_{0.74}Ga_{0.26}As$:Si	50 nm	5×10^{18}
Graded Buffer	$In_xGa_{0.26}As$:Si ($0.53 < x < 0.74$)	0.5 - 2.0 μm	5×10^{18}
Buffer	$In_{0.53}Ga_{0.47}As$:Si	300 nm	5×10^{18}
n+ Substrate	InP:Si		$2 - 5 \times 10^{18}$

Table 2. Matrix of parameters investigated in this study.

Parameter	Variation
Buffer Layer Thickness (μm)	0.5, 1.0, 2.0
Buffer Layer Growth Temperature (°C)	300, 350, 400
Active Layer Growth Temperature (°C)	300, 350, 400
Buffer Layer Structure	Linearly Graded, Linearly Graded and constant composition

The growths performed in Phase I may be divided in to three groups. The first group consisted of three samples where the buffer layer thickness was 1.0 μm and the growth temperature was varied from 300°C to 400°C. The second group consisted of six samples where the buffer layer thickness was varied from 0.5 to 2.0 μm, the active layer temperature was held at 400°C, and the buffer layer temperature was varied from 300°C to 400°C. These samples attempted to optimize separately the growth of the buffer and the active layers. The final

growth was a sample with a standard 1.0 μm linear grade followed by a 1.0 μm compositionally uniform n^+ buffer. Thus the total buffer thickness was 2.0 μm. This sample's buffer layer was grown at 350°C and its active layer at 400°C. Thus comparison with the 2.0 μm sample from the second set of growths illustrates the effect of varying the buffer structure. In addition, this sample permitted the formation of top-side and back-side contacts to investigate the presence of charge trapping centers in the device. The results of these three sets of growths will be discussed in the next sections.

3.1.2 Double crystal X-ray diffraction

Double crystal X-ray diffraction was performed on several samples. A representative X-ray diffraction spectrum is shown in Figure 1 for a sample from the second set of growths with a 2.0 μm buffer layer grown at 350°C and an active layer grown at 400°C. Note that the two main peaks correspond to the InP substrate and the thick InGaAs active layer. A broad feature associated with the linearly graded buffer layer is also visible. Measurements of both the asymmetric (115) and symmetric (400) reflections were performed to permit determination of the indium composition of the active layer as well as the relaxation of the buffer layer. The indium composition was found to be within ±2% of the targeted value of 74%. Lower buffer growth temperatures appear to allow more relaxation. For example, for samples with active layers grown at 400°C, a buffer temperature of 350°C produced a film that was more than 95% relaxed while growth at buffer temperatures of 400°C produced a film that was less than 87% relaxed. These substantial amounts of relaxation are consistent with reported results [1] for the growth of low temperature linearly graded are expected to produce stable, high quality devices.

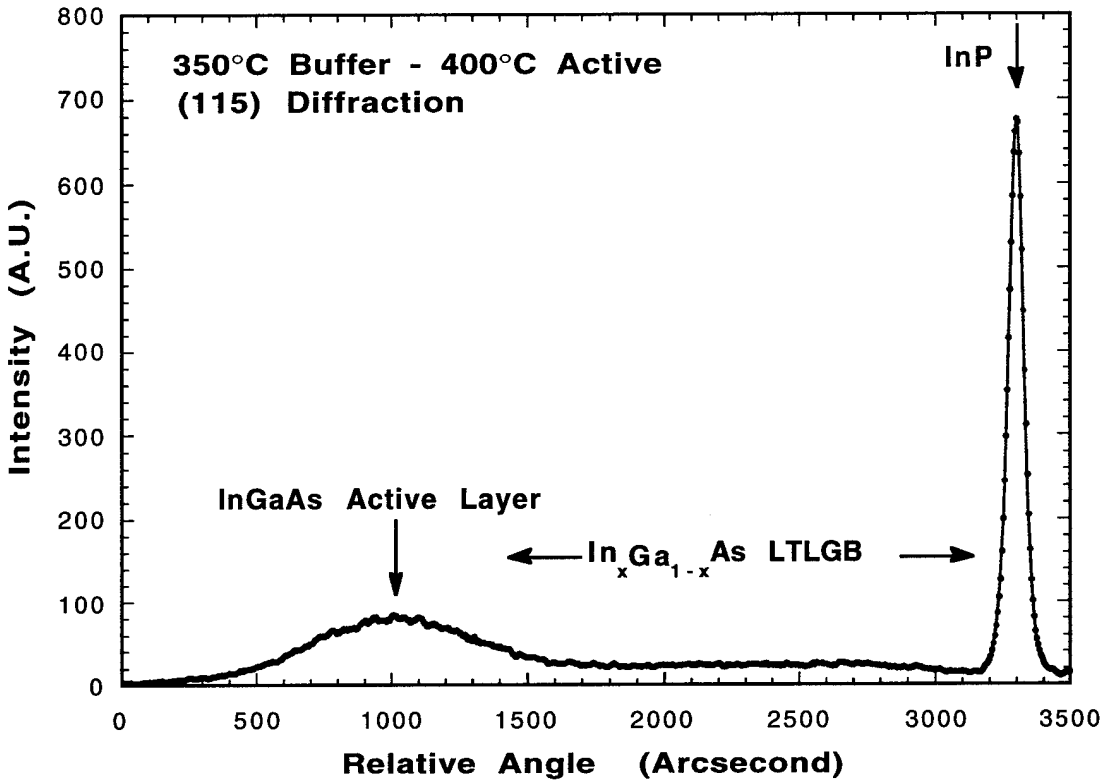


Figure 1. Representative double crystal x-ray diffraction spectrum.

3.1.3 Surface Morphology

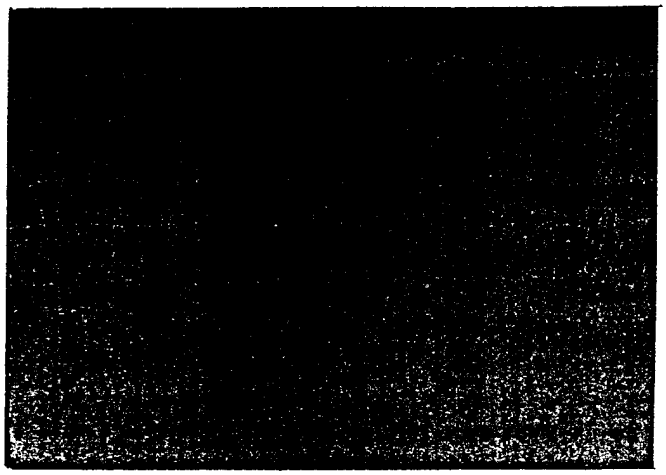
The surface morphology of the samples was examined using differential interference contrast (Nomarski) microscopy. As expected from highly-mismatched material, most of the samples exhibited visible crosshatching at the surface. Although not well understood, the presence of crosshatching seems to correlate well with the degree of relaxation in the active layer material [2]. A comparison of the Nomarski images for samples grown at buffer temperatures below 350°C with those grown at 400°C indicate that lower temperature buffers result in samples with more visible crosshatching. X-ray analysis performed on several of these samples demonstrated that those grown at 350°C are more relaxed than those grown at 400°C.

A closer inspection of the surface morphology of samples with 0.5 μm and 2.0 μm thick buffer layers that were grown at a buffer temperature of 350°C and an active temperature of 400°C, reveals that the slower grading rate results in larger separation between crosshatches. This is demonstrated clearly in Figures 2 and 3 that show Nomarski images of the samples grown at a buffer layer temperature of 350°C and an active layer temperature of 400°C. Similar observations have been

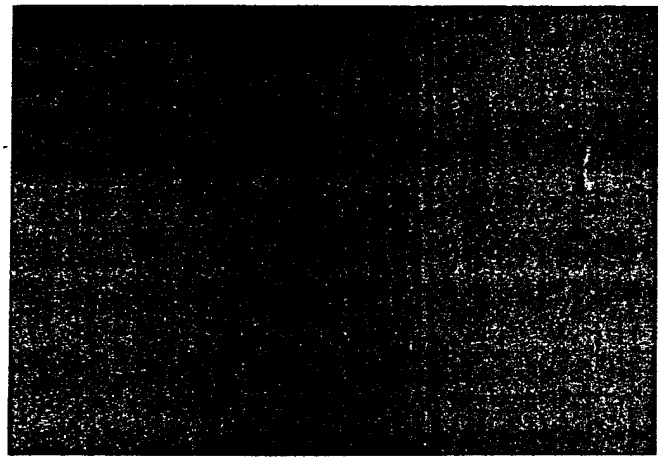
reported in the literature for mismatched growth of $In_{0.5}Ga_{0.5}As$ on GaAs [3]. Also shown in Figures 2 and 3 are the images of the sample with a 1.0 μm graded buffer followed by a 1.0 μm constant composition buffer. Unlike the samples with a standard buffer layer, no visible crosshatching was observed on this sample. Instead this sample has a very rough morphology. X-ray analysis of this sample, however, does indicate that it is more than 95% relaxed.

3.2 Fabrication of Mesa Diodes

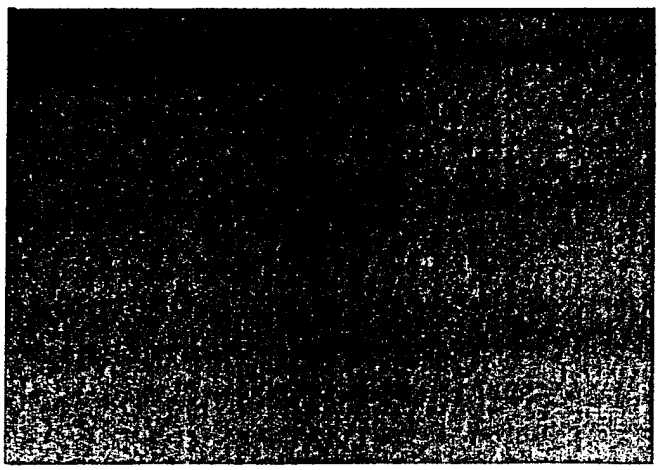
In order to quickly evaluate the electrical properties of the material, a mesa process was used to fabricate diodes ranging in size from 25×10^{-6} cm^2 to 1.6×10^{-3} cm^2. Although mesa processes are typically not used commercially due to an increase in the leakage current at the surface of the diode [4], developing a complete planar process would have slowed efforts at determining the suitability of this growth technique for use as 2.0-2.5 μm photo detectors. In order to eliminate the need for zinc diffusion and facilitate the use of a non-alloyed contact, a *p*–type cap structure was grown directly on top of the undoped active region. This consisted of a 100 nm *p*–type InGaAs layer, a 50 nm *p*-type InAlAs window, and a 50 nm p^+ cap doped at 5×10^{18} cm^{-3}. Following the growth, non-alloyed ohmic contacts were formed by lifting-off 1000 Å Ti/2500 Å Au. The diodes were isolated electrically by etching in H_3PO_4:H_2O_2:DI to a depth of 500 nm. A sketch of the resulting diodes is shown in Figure 4.



(a) 0.5 μm compositionally graded buffer.

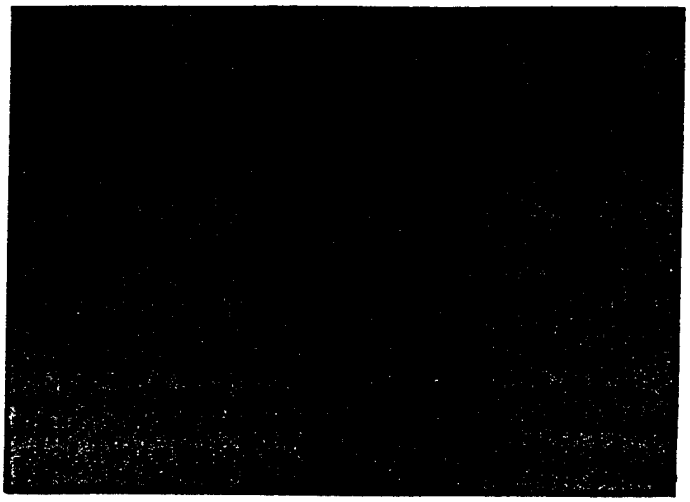


(b) 2.0 μm compositionally graded buffer.

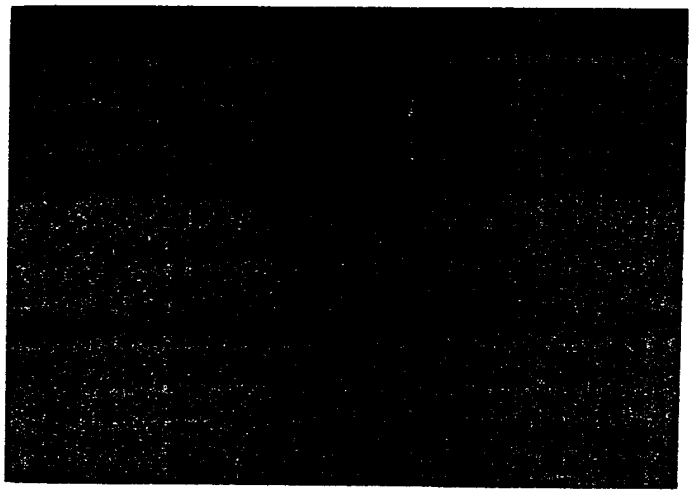


(c) 1.0 μm compositionally graded buffer + 1.0 μm constant composition buffer.

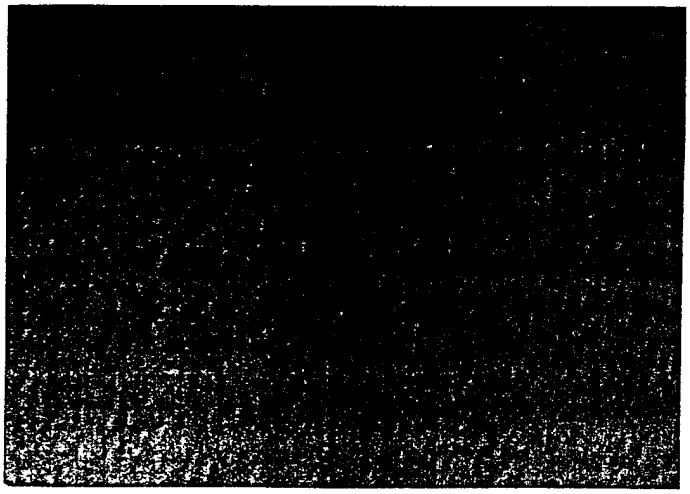
Fig. 2 Nomarski photographs (1000×) of samples grown at a buffer layer temperature of 350°C and an active layer temperature of 400°C.



(a) 0.5 μm compositionally graded buffer.



(b) 2.0 μm compositionally graded buffer.



(c) 1.0 μm compositionally graded buffer + 1.0 μm constant composition buffer.

Fig. 3 Nomarski photographs (1500×) of samples grown at a buffer layer temperature of 350°C and an active layer temperature of 400°C.

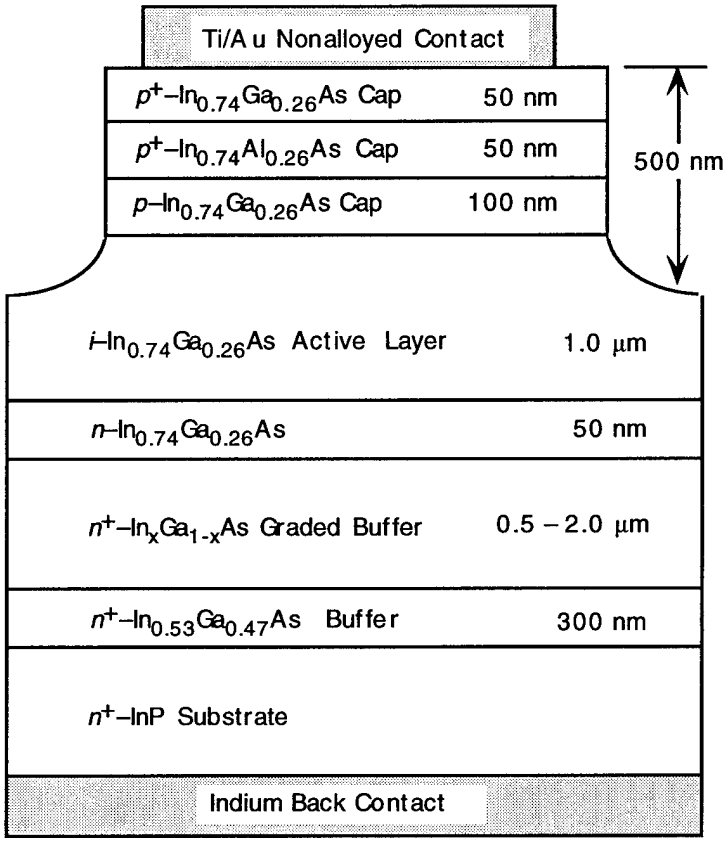


Figure 4. Mesa-isolated device structure

3.3 Fabrication of Planar Diodes

Sensors Unlimited's planar PIN diode process is summarized in Figure 5. In a typical PIN structure a thin (≤ 1 μm) short wavelength, lattice-matched $InAs_yP_{1-y}$ cap layer is grown on top of the $In_xGa_{1-x}As$ active layer to passivate the surface. Immediately upon receipt, wafers are coated with Si_3N_4. All subsequent processing occurs through holes in the Si_3N_4 so that all exposed surfaces of the final device are covered either by metal or dielectric.

The photodiodes are defined photolithographically and dry etching is used to open holes in the dielectric. The wafer together with pellets of ZnAs are sealed in an evacuated quartz ampoule and heated in a furnace. The ZnAs dissociates and the Zn is driven through the cap into the active layer doping both heavily p-type. The As over-pressure maintains the stoichiometry of the material.

After removal from the ampoule, the wafer is coated with a second layer of Si_3N_4 which also serves as an anti-reflective coating. Holes are opened in the AR coating and Au/Zn ohmic contacts are applied.

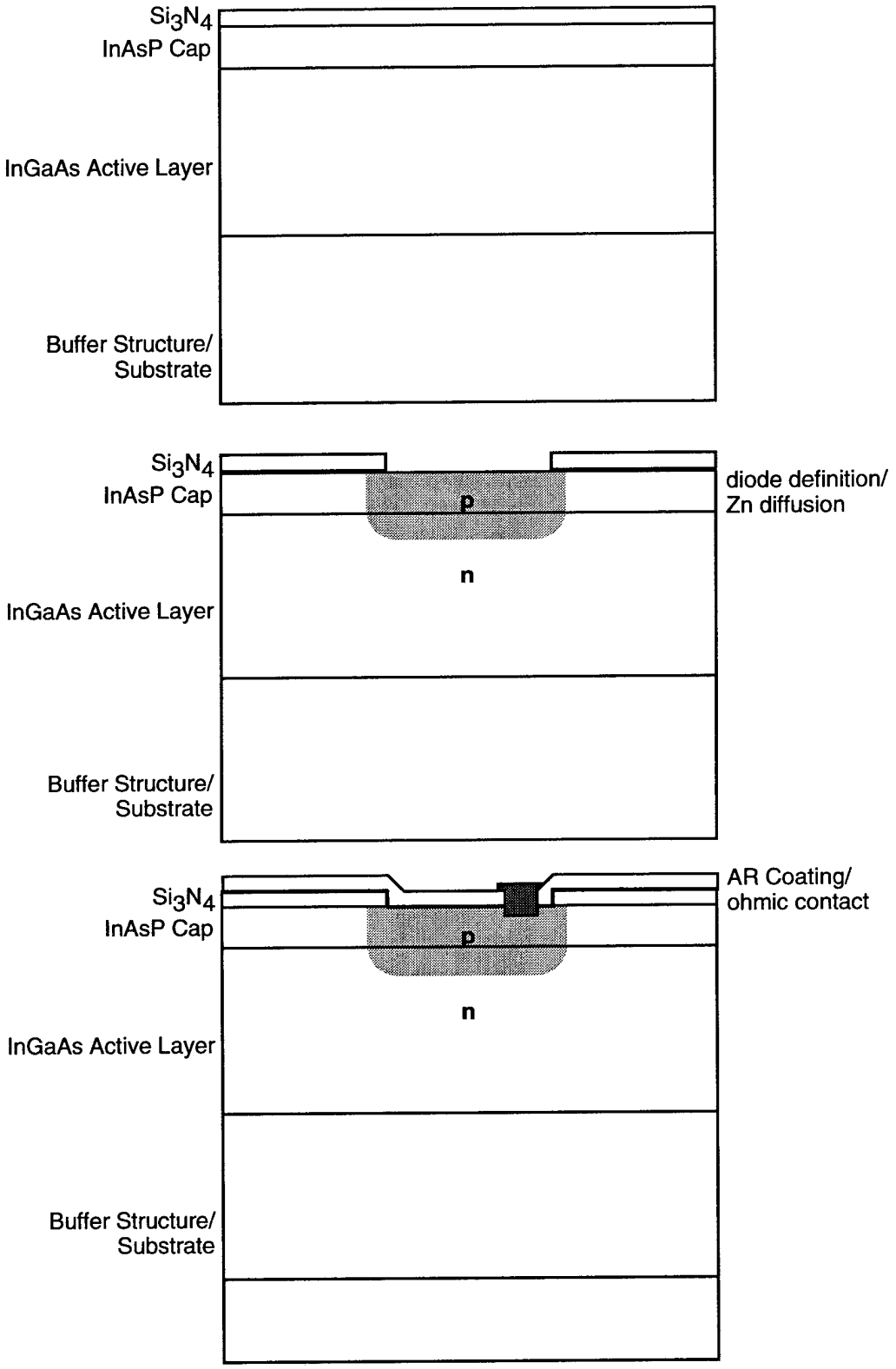


Figure 5. Sensors Unlimited's Planar PIN Process

3.4 Characterization of Mesa Diodes

3.4.1 Effect of Growth Temperature

In order to study the effect of growth temperature on device performance, the first group of samples was grown with a fixed buffer layer thickness of 1.0 μm and growth temperatures ranging from 300°C to 400°C. For all samples in this group, the substrate temperature was held at a constant value throughout the growth of the buffer and active layers. A comparison of the dark currents for 50 x 50 μm^2 diodes fabricated on samples grown at 300°C, 350°C, and 400°C is shown in Figure 6. The data presented in this figure demonstrates that the leakage current increases dramatically as the growth temperature is reduced from 400°C to 300°C. In particular, the current at a reverse bias of 1V ranges from approximately 50 nA for the sample grown at 400°C to more than 10 μA for the sample grown at 300°C. This represents more than a two order of magnitude increase in current as the growth temperature is reduced. For reference, exact values of zero-bias resistance-area product and dark current at voltages of -1V, -5V, and -10V are given in Table 3.

These data seem to indicate that higher growth temperatures result in material with superior electrical performance. This conclusion may be misleading, however, because the substrate temperature appropriate for growth of the active layer may not be suitable for growth of the buffer layer material. Therefore, these results suggest that the active layer growth temperature should be kept in the range of 400°C. In order to optimize the growth temperature of the buffer layer, a second group of samples was grown at an active layer temperature of 400°C. The characteristics of samples in this second group are described in the following section.

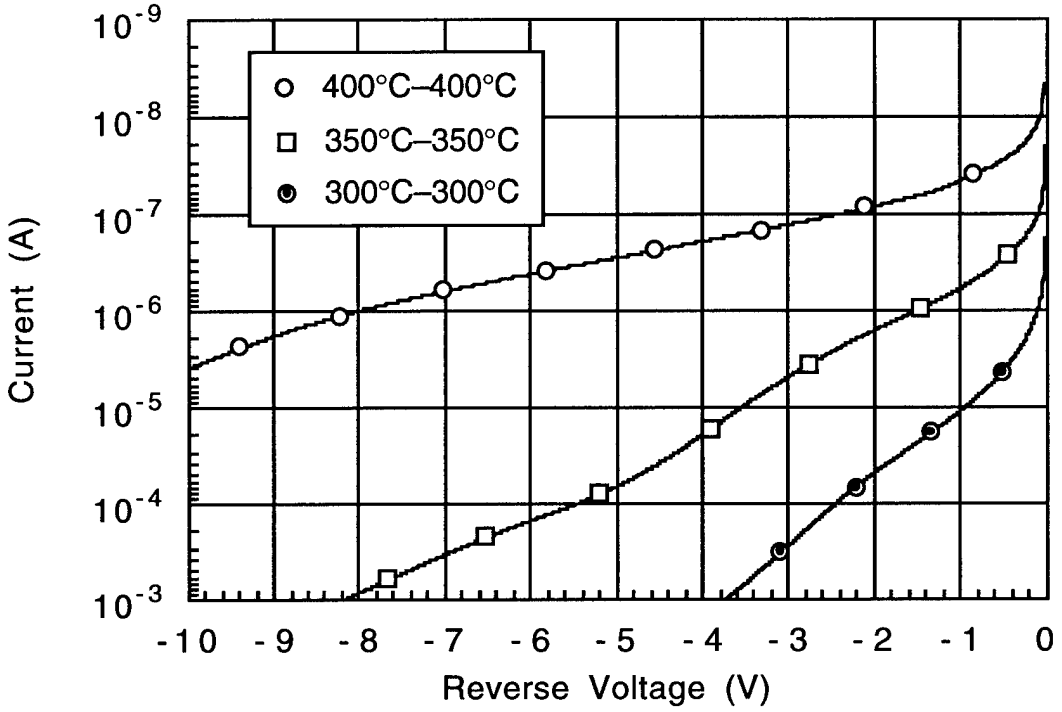


Figure 6. Typical I-V curves from 50× 50 μm^2 mesa-isolated diodes with 1.0 μm graded buffer layers.

Table 3. Electrical data from 50 × 50 μm^2 mesa-isolated diodes with 1.0 μm graded buffer layers.

Growth Conditions	1 μm buffer
300°C Buffer 300°C Active	I@-1V = 11.2 μA RoA = 2.6 Ω cm
350°C Buffer 350°C Active	I@-1V = 531 nA -5V = 180 μA RoA = 14.5 Ω cm
400°C Buffer 400°C Active	I@-1V = 47 nA -5V = 290 nA -10V = 4.1 μA RoA = 80 Ω cm

3.4.2 Effect of Buffer Layer Thickness and Growth Temperature

A second group of samples was compared to investigate the effect of buffer layer thickness and growth temperature on device performance. In this case, the buffer thickness was varied from 0.5 μm to 2.0 μm, the active layer temperature was held at 400°C, and the buffer layer temperature was varied from 300°C to 400°C. Typical dark current versus voltage curves for 50x50 μm^2 mesa-isolated diodes fabricated on samples with a 2.0 μm buffer layer are shown in Figure 7. Unlike the first group of samples where diodes grown at 400°C had the lowest dark currents, these curves demonstrate that a slight reduction in the buffer layer growth temperature (from 400°C to 350°C) can lead to further improvements in device performance.

In order to determine the effect of buffer thickness on device performance, a similar plot is shown in Figure 8 for diodes fabricated on samples with a 0.5 μm buffer layer. To assist with the comparison of devices grown at different buffer thicknesses, electrical data for both cases are summarized in Table 4. From these data, it is evident that diodes fabricated from samples grown at a buffer temperature of 350°C had the lowest dark current irrespective of buffer thicknesses. Moreover, although the shape of the I–V curves for these samples is somewhat different at intermediate voltages, the low bias and high bias current values do not depend significantly on the buffer thicknesses. This suggests that buffers thicknesses in the range of 1.0 μm should be sufficient to relieve the stain without generating an excessive number of threading dislocations that propagate through the active layer and degrade the device performance. This significant finding verifies earlier assumptions that lattice mismatched material suitable for device applications can be grown by MBE using very thin compositionally graded buffers.

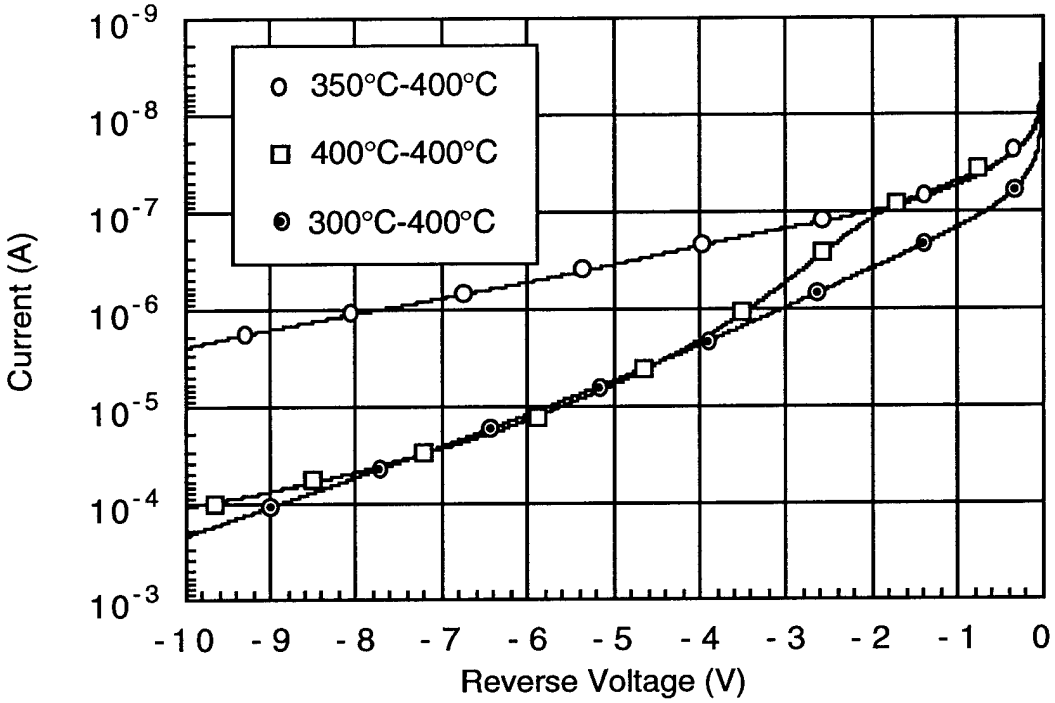


Figure 7. Typical I-V curves from 50 x 50 μm^2 mesa-isolated diodes with 2.0 μm graded buffer layers.

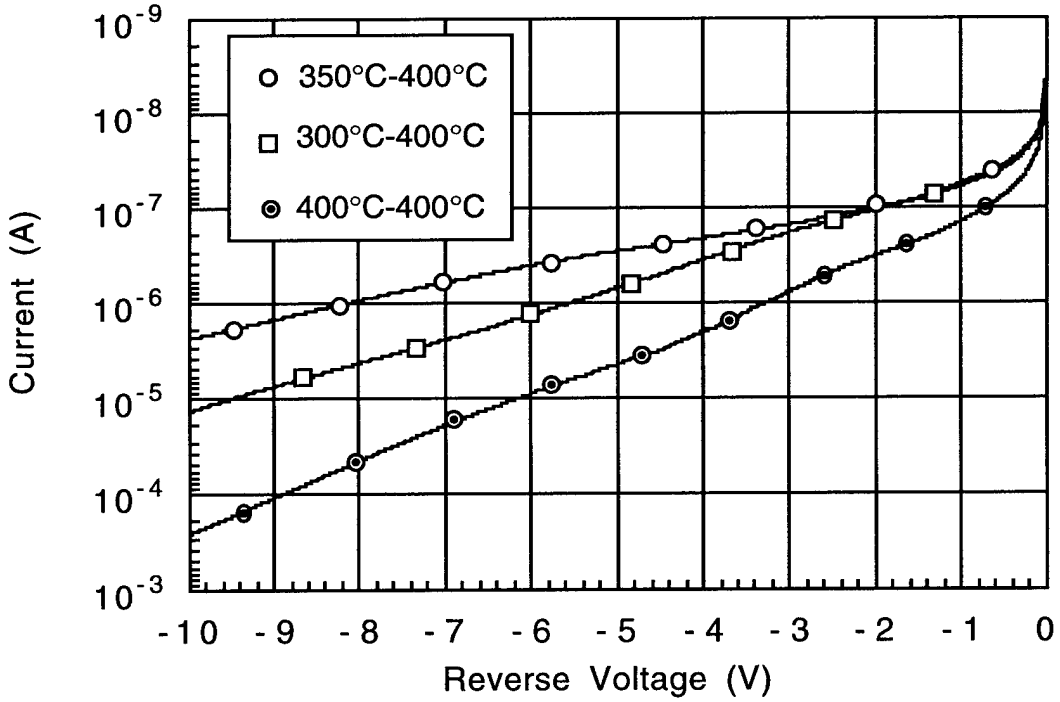


Figure 8. Typical I-V curves from 50 x 50 μm^2 mesa-isolated diodes with 0.5 μm graded buffer layers.

Table 4. Electrical data from 50 × 50 μm^2 mesa-isolated diodes with 0.5 and 2.0 μm graded buffer layers.

Growth Conditions	0.5 μm buffer	2 μm buffer
300°C Buffer 400°C Active	I@-1V = 150 nA -5V = 5.6 μA -10V = 220 μA RoA = 30 Ω cm	I@-1V = 62 nA -5V = 716 nA -10V = 14.1 μA RoA = 43 Ω cm
350°C Buffer 400°C Active	I@-1V = 55 nA -5V = 357 nA -10V = 2.5 μA RoA = 53 Ω cm	I@-1V = 57 nA -5V = 295 nA -10V = 2.4 μA RoA = 87 Ω cm
400°C Buffer 400°C Active	I@-1V = 50 nA -5V = 6.06 μA -10V = 112 μA RoA = 66 Ω cm	I@-1V = 145 nA -5V = 4.65 μA -10V = 269 μA RoA = 47 Ω cm

Additional characterization of the diodes from this group revealed that the dark current of several of the samples degrades rapidly with time. This is shown in Figure 9, where the current at a reverse bias of-5V is plotted as a function of time for diodes fabricated from samples grown at buffer temperatures of 300°C, 350°C, and 400°C. Although the diodes grown at lower buffer temperatures (350°C and 300°C) have the lowest initial current, after less than five minutes of operation their leakage current has exceed by a factor of four the current of the sample grown at a buffer temperature of 400°C.

Since the current degradation was very sensitive to the surface conditions (dry versus humid), the additional leakage current has been attributed to charge trapping at the mesa-isolated surface of the device (these devices were not passivated with Silicon Nitride prior to characterization). In order to verify that the charge trapping was not

occurring in the low-temperature graded buffer, a sample was grown with a modified buffer structure to facilitate both top-side and back-side n-type ohmic contact formation. In this way, if both topside contacts are used to measure the I-V characteristics of the diode, the current is confined to the active layer and does not flow through the low temperature buffer. The reverse I-V characteristics of the a topside device were identical to the characteristics of a p-type topside and an n-type backside device of the same size and thus confirms that the trapping is occurring primarily at the surface. Similar surface leakage problems also encountered on mesa-isolated photodiodes grown using VPE material. The surface leakage was virtually eliminated in VPE photodiodes by using a planar process rather than a mesa process.

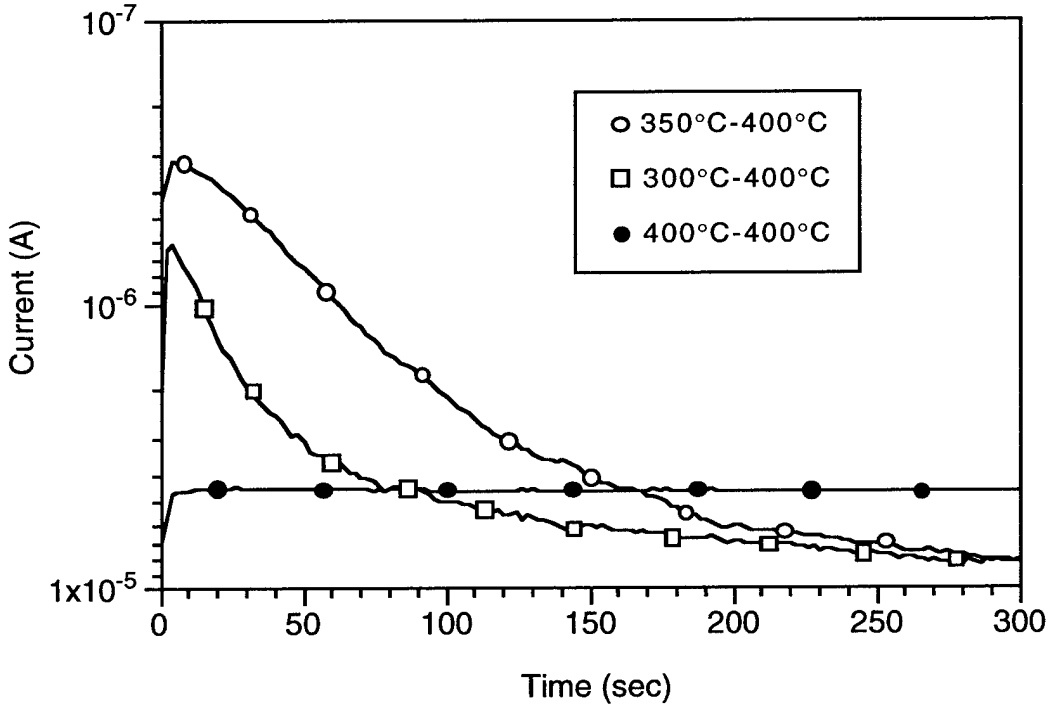


Figure 9. Current versus time for 50 x 50 μm^2 mesa-isolated diodes with 2.0 μm graded buffer layer.

3.4.3 Variation of Buffer Layer Structure

The effect of buffer layer structure on device performance was studied by comparing a sample with a 2.0 μm graded buffer grown at 350°C to a sample with a modified buffer layer. The modified structure consisted of a standard 1.0 μm compositionally graded buffer followed by a 1.0 μm compositionally uniform n^+ buffer layer. The electrical data for devices fabricated from these two samples is summarized in Table 5.

Although the R_0A products are nearly equal, the dark current at large reverse biases is substantially lower for the sample with the modified buffer structure. This would suggest that the effectiveness of the compositionally graded buffer in trapping dislocations can be affected greatly by the structure of the material grown on top (compositionally uniform buffer, active layer thickness, etc.).

Table 5. Electrical data from 50 × 50 μm^2 mesa-isolated diodes with 2.0 μm total thickness buffer layers.

Growth Conditions	1 μm Linearly Graded + 1 μm Constant Composition Buffer	2 μm Linearly Graded Buffer
350°C Buffer 400°C Active	I@-1V = 47 nA -5V = 162 nA -10V = 567 nA RoA = 75 Ω cm	I@-1V = 57 nA -5V = 295 nA -10V = 2.4 μA RoA = 87 Ω cm

The complications in this program result from the difficulty in growing phosphorous-containing compounds by MBE. It was decided, therefor, that the passivation cap should be lattice-matched, short wavelength $In_xAl_{1-x}As$. From electrical and optical perspectives, the choice appears to have no consequences. From a processing perspective, however, significant recalibration of the Zn diffusion step must be carried out.

The Zn needs to be driven through the cap to a controlled depth in the active layer. With $InAs_yP_{1-y}$ caps, the required times and temperatures are well calibrated as functions of cap thickness and cap and active layer compositions.

Diffusion through $In_xAl_{1-x}As$ will require an entire new set of calibrations. While straight forward, it is a tedious procedure. For commercial device, it is a necessary step for the sake of device performance, lifetime, and ability to fabricate diode arrays. Given the excellent results on the mesa diodes with the grown-in p-n junctions, it was decided to postpone this task until Phase II.

3.4.4 Characterization of Photodiodes

As was discussed above, the optimum structure consists of a 1 μm tick LTLGB structure grown at 350°C with a 1 μm n+ In.74Ga.26As buffer layer to reduce the effects of charge trapping at the LTLGB/active layer interface. The final growth of the Program is summarized in Table 6.

Table 6. Structure of final growth

Layer	Material	Thickness	Doping (cm^{-3})
Contact	$In_{.74}Ga_{.26}As$:Be	500 Å	$5x10^{18}$
Cap	$In_{.74}Al_{.26}As$:Be	500Å	$5x10^{18}$
p+	$In_{.74}Ga_{.26}As$:Be	1000Å	$6x10^{17}$
n- Active	$In_{.74}Ga_{.26}As$	1.0 μm	undoped
n+ Buffer	$In_{.72}Ga_{.26}As$:Si	1.0 μm	$5x10^{18}$
LTLGB	$In_xGa_{1-x}As$:Si ($.53 < x < .74$)	1.0 μm	$5x10^{18}$
Buffer	$In_{.53}Ga_{.47}As$:Si	3000 Å	$5x10^{18}$
n+ Substrate	InP:Si		$2\text{-}5x10^{18}$

Mesa photodiodes were fabricated using a mask set provided by Sensors Unlimited. The photodiodes were "snowman" structures with 100 μm diameter optically active areas and 25 μm diameter ohmic contacts. The total active area is $8.3x10^{-5}$ cm^2. The wafer was probed for room temperature shunt resistance. A representative diode was mounted on a two stage thermoelectric cooler in a hermetically-sealed TO-37 package.

The devices were characterized both for the room temperature spectral response (Figure 10) and the temperature dependence of RoA (Figure 11). The temperature dependence of RoA is replotted as ln(RoA) vs. 1/T in Figure 12 indicating a diode quality factor $n \approx 1.2$. These results, as compared to commercial VPE material are discussed further in Section 3.6.

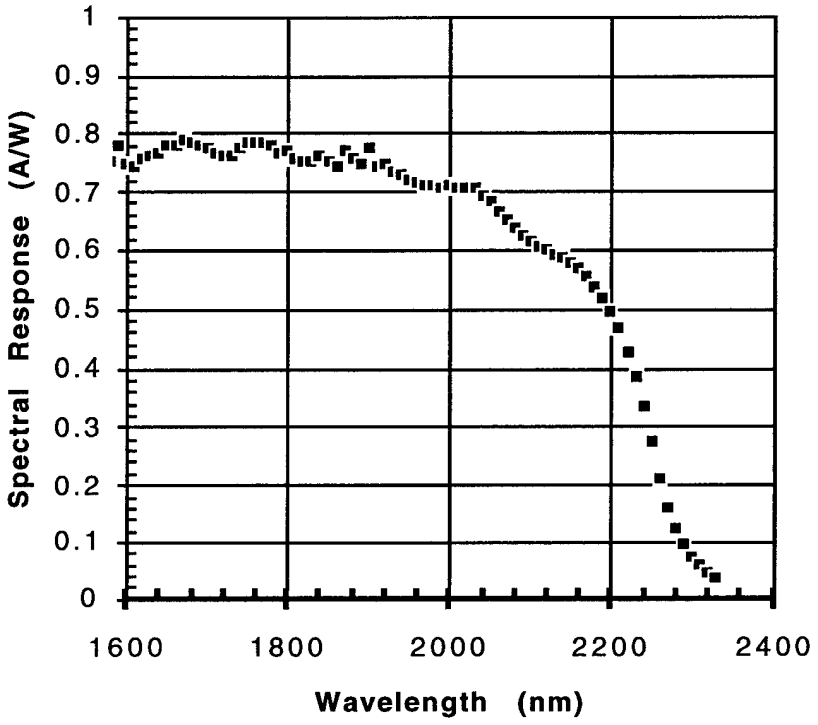


Figure 10. Room temperature spectral response of final growth

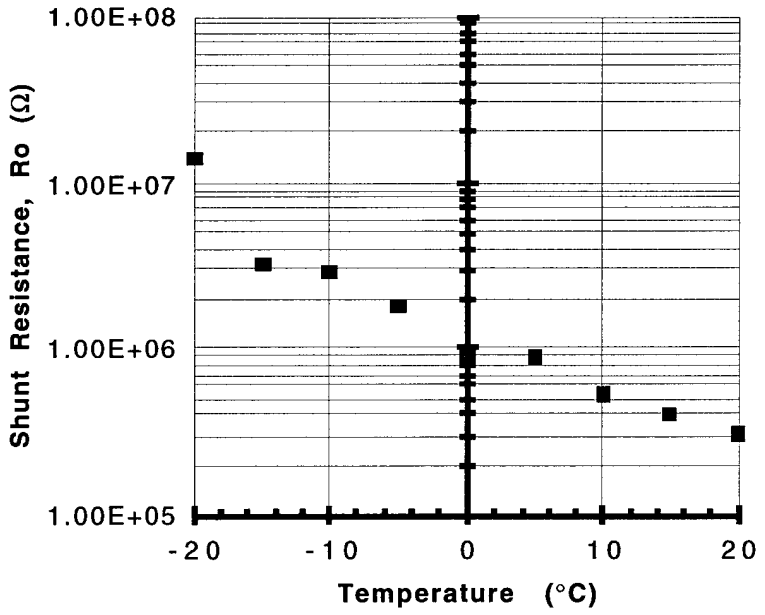


Figure 11. Temperature dependence of shunt resistance

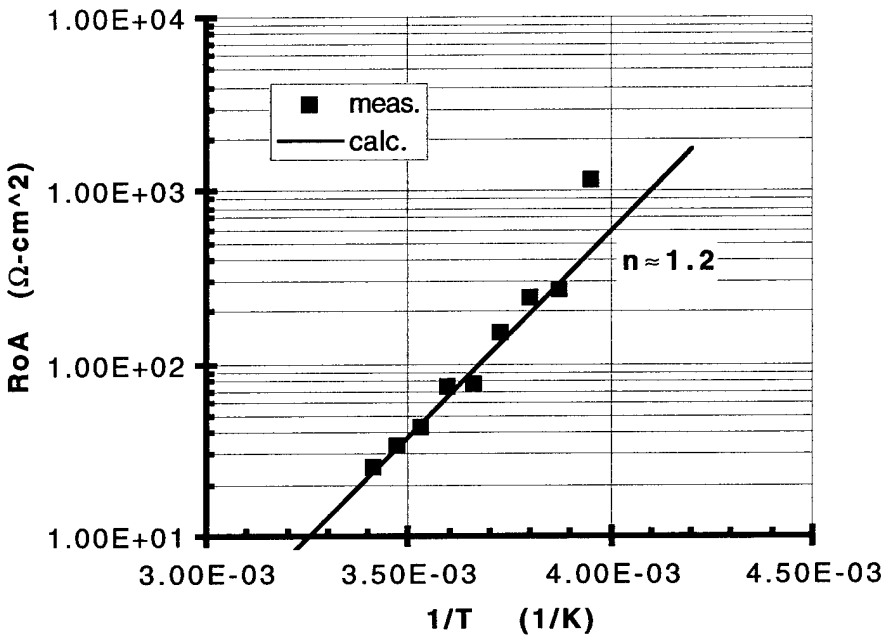


Figure 12. Temperature dependence of RoA

3.5 Substrate Temperature Control Improvements

The electrical and optical characteristics of the material demonstrate clearly that the substrate temperatures required to grow device quality material with a very high indium composition are lower than those traditionally used for GaAs or $In_{0.53}Ga_{0.47}As$. Our best results were obtained with temperatures from 350°C to 400°C. Present day commercial MBE systems typically use a thermocouple for feedback control and an optical pyrometer for calibration. Unfortunately, because of the small amount of radiation emitted from the sample, optical pyrometers are not usable below 500°C. Because thermocouples are not usually mounted directly on the substrate, their temperature readings are not true indications of the substrate temperature. Therefore, the accuracy of substrate temperature measurement using standard techniques is very poor at the temperatures needed for growth of the materials in this study.

We have designed an improved temperature control system which uses backside reflectance spectroscopy but avoids the interference problems encountered when measuring the bandgap by instead measuring the E_1 critical point to determine temperature. Because the E_1 critical point is at a higher energy than the bandgap, its penetration depth is smaller, and no light used for measuring is expected to be transmitted to

the front of the substrate. E_1 is also better defined in the reflectance spectrum[1] so it can be measured more easily than the bandgap [5], E_0.

The theoretical and experimental temperature dependence of the E_1 critical point has been studied [6,7]. At temperatures greater than room temperature, $E_1(T)$ is approximately linear making its derivative a constant. We have measured the E_1 critical point of S.I. and n^+ GaAs and InP substrates using reflection spectroscopy. The reference cell is an Al coated mirror. The sample is indium bonded to the end of a resistive heater rod whose temperature can be varied. The sample's temperature is measured by a thermocouple at the end of the rod. The quartz-halogen light source is focused through a scanning monochrometer and onto a chopper. This chopper is comprised of three sections: opaque, mirror, and transparent. If the monochromatic light strikes the opaque portion of the chopper, no light is incident on the reference or sample cells and the amplitude of the dark current is measured. When the light from the monochrometer strikes the mirrored surface of the rotating chopper, light is directed onto the reference cell where the intensity of the light at that wavelength is measured at the photomultiplier tube (PMT). When the monochromatic light passes through the clear section of the chopper, light is directed onto the sample cell and its intensity is measured at the PMT. The percent reflectance for a given wavelength is specified as a percentage relative to the reference cell.

Our design for a prototype system for temperature control within the MBE uses remote optics from within the ultra-high vacuum (UHV) chamber which has the advantage of being away from the high temperature environment of the substrate. Other systems use a rod mounted just behind the substrate. This approach, while providing a better signal to noise ratio, can be risky because of the higher potential of material from the sources building up on the surface of rod, eventually rendering it useless as an optical device. Thus, we believe that our approach will provide better long term reliability.

Our system works by shining white light through one leg of a bifurcated fiber bundle, through the UHV feedthrough, and onto the end of a single fiber within the chamber. This single fiber routes the light to its transmitting/receiving end. The light is focused through a lens and onto a 45° mirror where the light travels down a hollow tube to the substrate. The light reflects off the back of the substrate, through the tube, off the mirror, through the lens and onto the end of the same fiber. This reflected light travels through the single fiber and the feedthrough onto the fiber bundle where 50% of the signal goes back to the light source and 50% to

the spectrometer where the spectral content of the reflected light is measured to determine the position of E_1 and hence, the temperature of the substrate.

3.6 Comparisons with Commercial VPE Material

The driving force behind this Program is the need for a source of high quality extended wavelength InGaAs PIN diode structures for large area devices such as linear and area near infrared focal plane arrays. The current state-of-the-art is produced by VPE with Sumitomo in Japan as the only commercial supplier. The material in nonuniform and not very well suited for large devices. Our goal is develop MBE as a source of both high quality and commercially viable material. We believe we have exceeded in our Phase I objective of demonstrating the feasibility with 2.2 μm cutoff material.

Figure 13 compares the epitaxial structure of Sumitomo VPE material with the optimum structure developed during Phase I. The buffer structure of the MBE material is only 2 μm thick compared with 13 μm in the VPE material. This decrease is critical as MBE growth rates are only about 1 μm per hour and this result greatly enhances the opportunities for commercialization.

It is important to note three critical differences. The MBE material contains a grown-in p-n junction as we have not yet developed a planar process for zinc diffusion through the InAlAs cap. The thickness control of MBE allows a much thinner cap which enhances the short wavelength response of frontside illuminated devices. Finally, during Phase I, the MBE active layers were only 1 μm thick and did not incoporate an anti-reflective coating. This suppressed the long wavelength response but is only an artifact of the geometry, not the material quality.

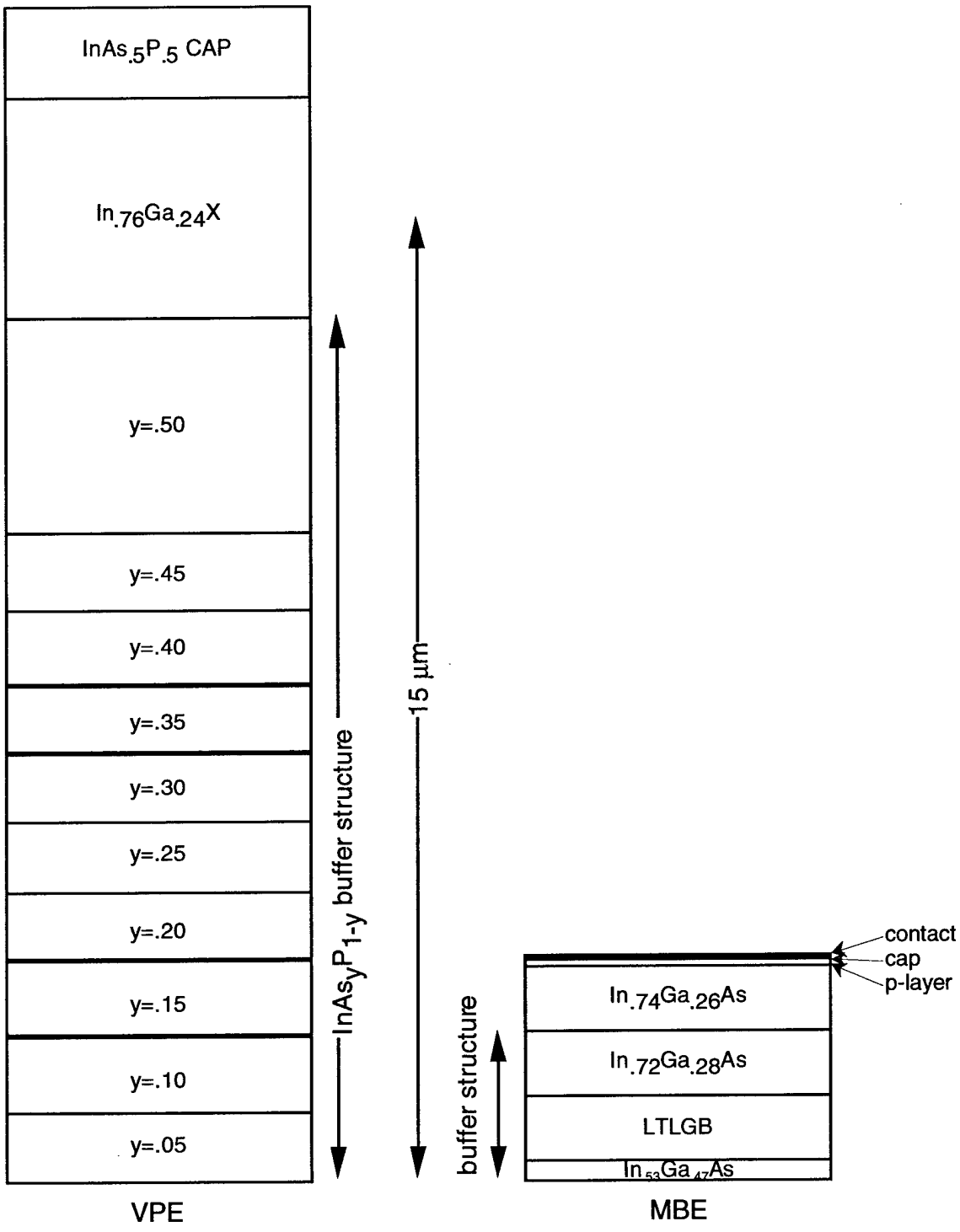


Figure 13. Epitaxial structures of MBE and VPE wafers

PIN diodes in extended InGaAs are generally operated at zero-bias. The critical electrical parameter is thus the shunt resistivity, RoA. For staring devices, it is common to operate at reduced temperatures to make longer integration times possible. The temperature dependence of RoA is also important and can be characterized by the diode quality factor, n. n ranges from 1 to 2 and the lower the value the stronger the increase in RoA with decreasing temperature.

Figure 14 is the temperature dependent RoA of an MBE PIN diode compared to a VPE device. The absolute value of the VPE material at 20°C, 145 Ω-cm^2, is about 8 times greater than that of the MBE material, 25 Ω-cm^2. Value across the MBE wafer ranged from 15-75 Ω-cm^2. While not negligible, the difference likely results from unpassivated edge currents in the mesa-isolated MBE diode. The MBE device <u>does</u> exhibit a lower diode quality factor (less than 1.2 vs. more than 1.3). We feel that the MBE devices will be electrically equivalent to the VPE devices after the development of the planar process in Phase II.

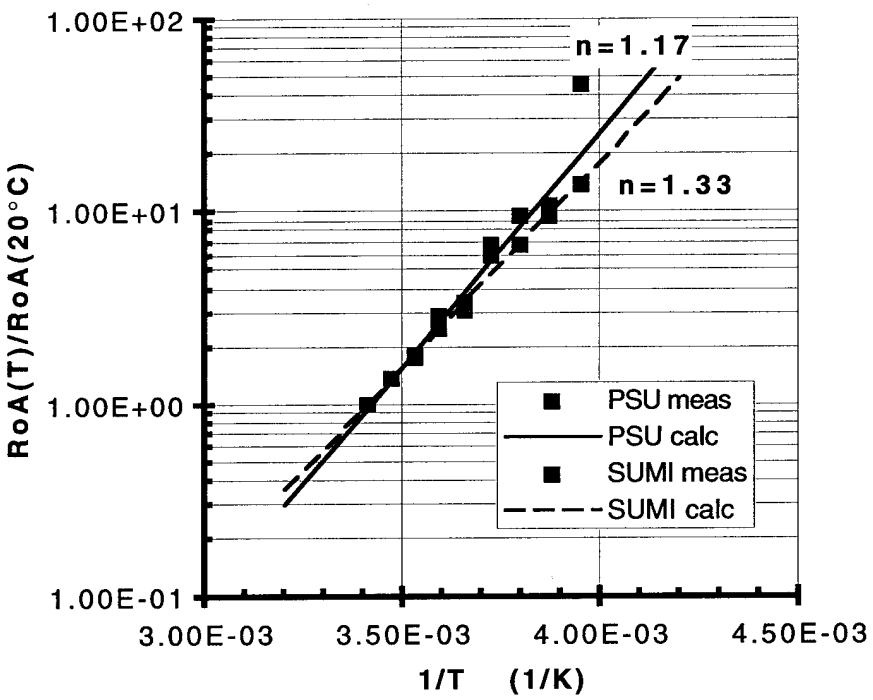


Figure 14. Shunt resistivity of MBE and VPE PIN diodes

Finally, Figure 15 compares the spectral response of the MBE diode with that of the VPE device. As expected, the short wavelength response is equivalent. At long wavelength, much of the photons striking the MBE diode with its 1 μm active layer are absorbed in the buffer structure reduce the response. This effect is geometric rather than physical and, during Phase II we will produce full 4 μm thick active layers.

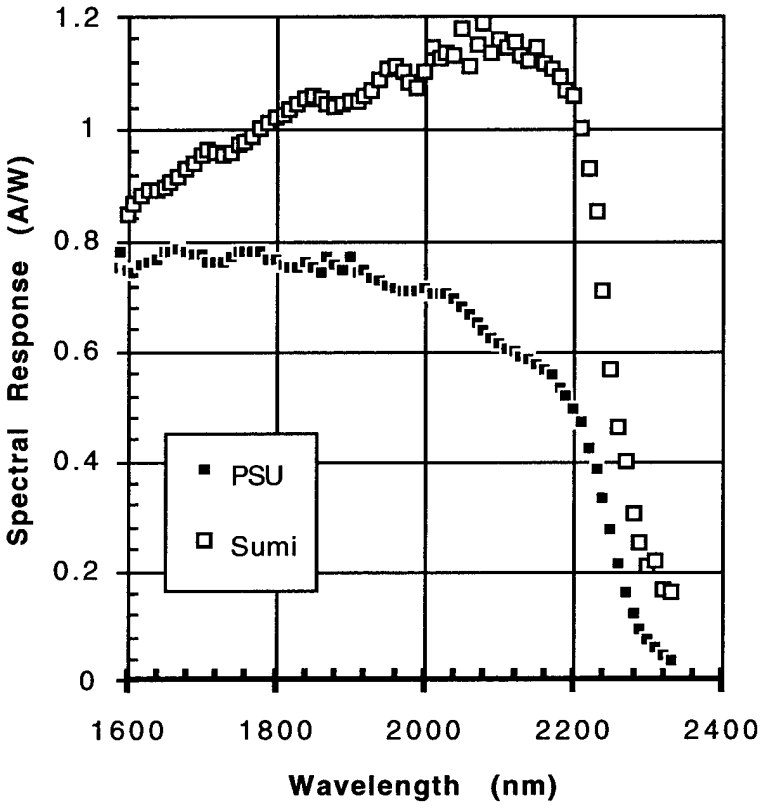


Figure 15. Spectral response of MBE and VPE PIN diodes

4. Assessment of Technical Feasibility

The goal of this Program is to develop MBE as a commercial alternative to VPE for lattice-mismatched, extended wavelength InGaAs PIN diodes. There primary motivations is that VPE is difficult to control and fundamentally nonuniform. Wafer yield (proportion of grown wafers that are usable) tends to be low and within acceptable wafers, devices must be culled from "sweet spots." We hope to take advantage of the fundamental large area uniformity of MBE.

A number of obstacles stood in the way:

- The VPE buffer structure is 10-12 μm thick. With its 1 μm growth rate, this would make MBE impractical.

- Conventional wisdom is that during such long growth periods, bad things happen. Even if commercially acceptable, it has been believed that MBE cannot grow high quality lattice mismatched minority carrier device structures.

Our Phase I Program accomplished its goal of demonstrating technical feasibility using material with a 2.2 μm cutoff. Specifically:

- The short wavelength (1.6-1.7 μm) **spectral response of 0.8A/W** is equivalent to that observed with the best VPE material. The somewhat lower longer wavelength response is due to the thinner (1 μm vs. 4 μm) active layer.

- The room temperature **RoA product of 25 Ω-cm^2** is reasonable close to the 100-200 typically observed with the best VPE material. We believe that the difference is primarily due to the mesa structure which adds leakage current from the exposed junction at the mesa edge.

- The temperature dependence of RoA is a clean exponential with a **diode quality factor of n ≈ 1.2.**

All of these results indicate that it is feasible to grow lattice mismatched InGaAs PIN structures with performance equivalent to VPE.

5. Summary of Planned Phase II Activity

While we are very encouraged that we accomplished all of the goals in our Phase I proposal, as we anticipated then, much remains to be done during Phase II. The Phase II Work Statement will be divided into 4 major categories:

1) The indium content of the InGaAs active layer must be increased from 74% to 82%. This will extend the long wavelength response from 2.2 to 2.6 μm.

2) The zinc diffusion process most be modified and calibrated to allow planar processing through the InAlAs cap layer.

3) The LTLGB structure used in Phase I was gown in InGaAs. These layers will block much of the light when used with backside-illuminated devices such as two-dimensional focal plane arrays. During Phase II, a transparent InAlAs LTLGB buffer will be developed.

4) A non-invasive optical monitoring technique will be developed to better control the relatively low (≈ 350°C) growth temperatures used for the buffer structure.

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"Development of MBE Growth Techniques for High Quality 1.5 - 2.5 μm Near Infrared Sensing Devices"

Addendum To Final Report

Contract #: N00014-94-C-0262

Period: October 1, 1994 through March 31, 1995

SUMMARY

An abstract based on this Phase I work was submitted to the 1995 Electronic Materials Conference to be held in Virginia in June 1995. A verbatim copy of this abstract with its supplementary figures is attached as a complete addendum to our final report.

Molecular Beam Epitaxy of $In_{0.74}Ga_{0.26}As$ on InP for Near-Infrared Detectors

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Operation of detectors in the near-infrared (1.0 – 2.5 μm) is attractive for a variety of applications including environmental remote sensing, night vision, and blood glucose level monitoring. However, currently available material grown by vapor phase epitaxy (VPE) suffers from compositional nonuniformities that make the fabrication of large-area detector arrays difficult. In this work we used molecular beam epitaxy (MBE), which offers the advantage of excellent uniformity, to grow $In_{0.74}Ga_{0.26}As$ active layers on InP substrates. To permit the growth of high quality epitaxial layers with such a large mismatch to the substrate (1.4%), a linearly graded buffer layer was used. Such buffers have been shown to minimize problems from threading dislocations[1]. Here, we investigated the effect of varying the growth temperature and thickness of the buffer layers on the material quality. The samples were compared using current–voltage measurements, 300 K optical transmission, and double crystal x-ray diffraction.

The structure for all samples consisted of a 3000 Å lattice matched n^+–InGaAs buffer followed by a linearly graded region, a 500 Å n^+–$In_{0.74}Ga_{0.26}As$ layer, a 1 μm undoped $In_{0.74}Ga_{0.26}As$ active region, and a 3000 Å p^+–cap layer. The indium composition in the linearly graded region was increased from 53% to 74% and the rates were varied from 10% In/μm to 40% In/μm resulting in buffer thicknesses of 0.5 μm – 2.0 μm. Moreover, at each grading rate, the growth temperature was varied from 300°C to 450°C. Following the growth, the samples were processed into mesa-isolated diodes ranging in size from 50 μm to 1000 μm on a side .

Measurements of the reverse biased dark current reveal that, at low biases, samples grown at 400°C result in devices with superior electrical performance. As the growth temperature is lowered, the devices suffer from a severe degradation in the current as a function of time. This may be attributed to charge trapping, however, at this time it is not clear whether this occurs primarily at the mesa-isolated edge or in the bulk. As the growth temperature is raised, the breakdown characteristics improve but the low-bias dark currents become slightly higher. The dark current density at a 1V reverse bias for the material grown at 400°C is approximately $2mA/cm^2$. This compares favorably with commercially available VPE material that has dark current densities in the range of 20 mA/cm^2 at –1V. Moreover, optical transmission confirmed that the wavelength cutoff for this sample is approximately 2.2 μm. These results clearly demonstrate that MBE, which should offer improved compositional uniformity over VPE, can be used to produce material that is suitable for detector applications near 2.2 μm.

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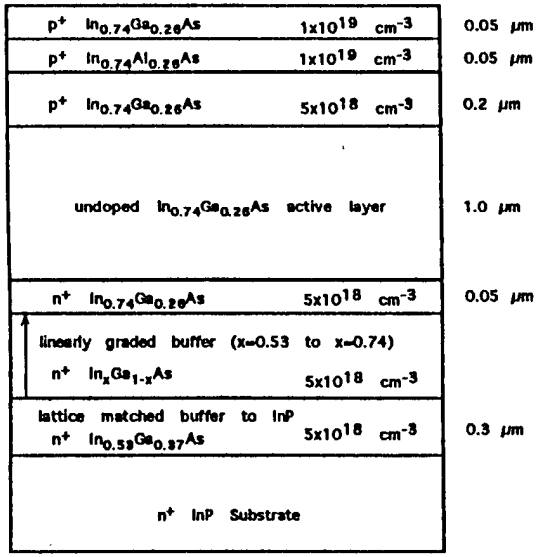
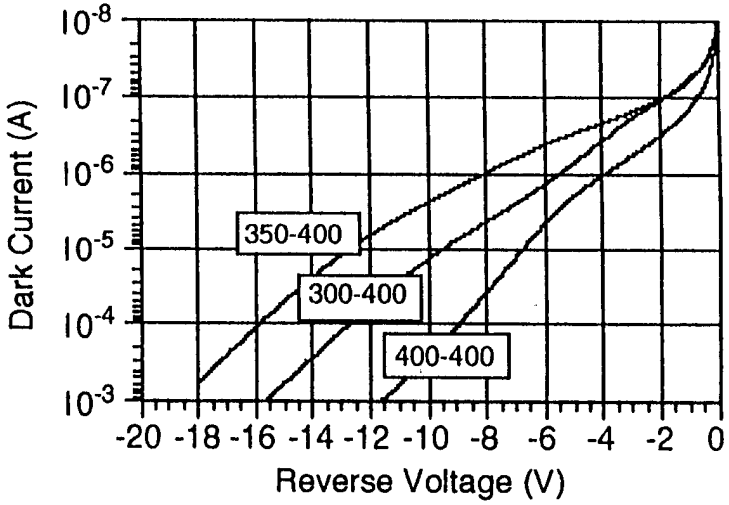
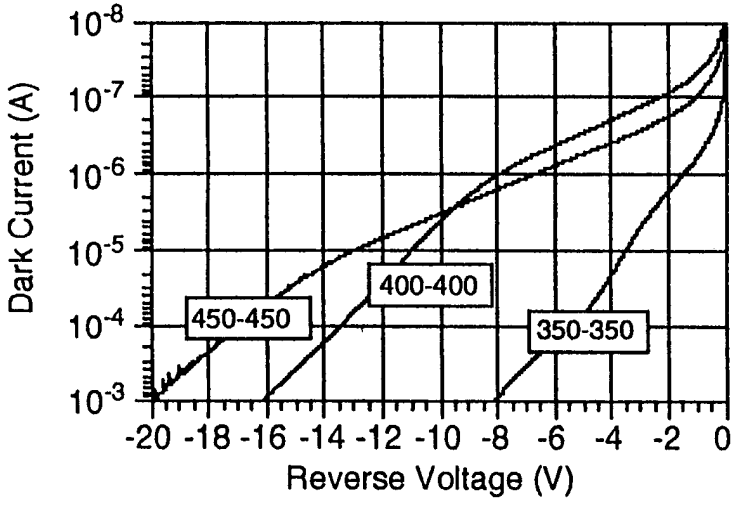
**This work was supported by the Navy through STTR Contract # N00014-94-C-0262.



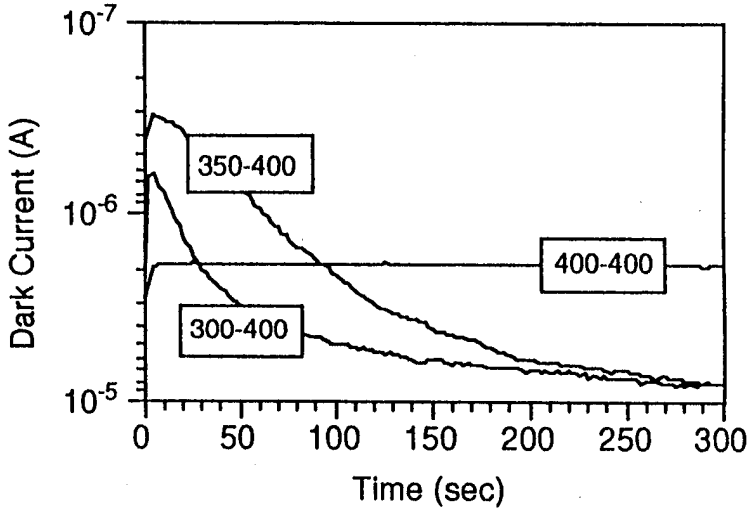
Structure grown using MBE. The growth rate of the linearly graded buffer was varied from 10% In/μm to 40% In/μm. The growth temperature was varied from 300 C to 450 C.



Dark current versus voltage for 50x50μm^2 devices at 300 K. In the legend, the first value corresponds to the growth temperature of the buffer while the second value corresponds to the growth temperature of the active layers. All devices have 2.0 μm thick buffers. Although the sample labeled 350-400 appears to have the lowest reverse dark current, the current degrades rapidly with time.



Dark current versus voltage for 50x50μm^2 devices at 300 K. In the legend, the first value corresponds to the growth temperature of the buffer while the second value corresponds to the growth temperature of the active layers. All devices have 1.0 μm thick buffers.



Dark current versus time for a 5V reverse bias. The 400-400 sample shows no degradation with time whereas the dark current for the 350-400 and 300-400 samples increases by over one order of magnitude in less than five minutes.